**ALU: (7 control bits)**

I/P: alu\_a, alu\_b;

O/P: alu\_c, alu\_z, alu\_out

Controls:

|  |  |  |
| --- | --- | --- |
| aluop\_1 | aluop\_2 | Operation |
| 0 | 0 | add |
| 0 | 1 | Subtract |
| 1 | 0 | Nand |

ALU inputs:

Alu\_a\_Mux:

|  |  |  |
| --- | --- | --- |
| alua\_1 | alua\_2 | input |
| 0 | 0 | PC |
| 0 | 1 | T1 |
| 1 | 0 | T2 |
| 1 | 1 | ir\_0-8->SE9 |

|  |  |  |  |
| --- | --- | --- | --- |
| alub\_1 | alub\_2 | alub\_3 | input |
| 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 |
| 0 | 1 | 0 | t2 |
| 0 | 1 | 1 | t3 |
| 1 | 0 | 0 | ir\_0-5->SE6 |
| 1 | 0 | 1 | ir\_0-8->SE9 |

**RF: (10 control bits)**

I/P : rf\_a1, rf\_a2, rf\_a3, rf\_d3

O/P: rf\_d1,rf\_d2

Controls:

rf\_en (active high)

|  |  |  |
| --- | --- | --- |
| r7wr\_1 | r7wr\_2 | Mux\_rf\_7 o/p |
| 0 | 0 | rf\_d3 |
| 0 | 1 | PC |
| 1 | 0 | t2 |
| 1 | 1 | alu\_out |

RF\_a1 input:

|  |  |  |
| --- | --- | --- |
| rf\_a11 | rf\_a12 | Mux\_rf\_a1 o/p |
| 0 | 0 | ir\_9-11 |
| 0 | 1 | 111 |
| 1 | 0 | t4 |
| 1 | 1 | Don’t caret |

RF\_a3 input:

|  |  |  |  |
| --- | --- | --- | --- |
| rf\_a31 | rf\_a32 | rf\_a33 | Mux\_rf\_a3 o/p |
| 0 | 0 | 1 | ir\_3-5 |
| 0 | 1 | 0 | 111 |
| 0 | 1 | 1 | ir\_6-8 |
| 1 | 0 | 0 | ir\_9-11 |
| 1 | 0 | 1 | t4 |

RF\_d3 input:

|  |  |  |
| --- | --- | --- |
| rf\_d31 | rf\_d32 | Mux\_rf\_a1 o/p |
| 0 | 0 | t1 |
| 0 | 1 | Ir0-8 -> Lshift 7 |
| 1 | 0 | t3 |
| 1 | 1 | Don’t care |

**Mem**: (5 control bits)

mem\_Write\_bar(active low)

mem\_read\_bar(active low)

Mem\_a mux:

|  |  |  |
| --- | --- | --- |
| mem\_a1 | mem\_a2 | mem\_a\_mux o/p |
| 0 | 0 | Pc |
| 0 | 1 | t1 |
| 1 | 0 | t2 |
| 1 | 1 | Don’t care |

Mem\_d (when write bar is 0)

mem\_d1:

0->t1

1->t3

**Reg T1: (3 control bits)**

en\_t1: Active high

|  |  |  |
| --- | --- | --- |
| t1\_1 | t1\_2 | t1\_mux o/p |
| 0 | 0 | rf\_d1 |
| 0 | 1 | alu\_out |
| 1 | 0 | mem\_d |
| 1 | 1 | Don’t care |

**Reg T2:(4 control bits)**

en\_t2: Active high

|  |  |  |
| --- | --- | --- |
| t2\_1 | t2\_2 | rf\_t2\_mux o/p |
| 0 | 0 | rf\_d2 |
| 0 | 1 | alu\_out |
| 1 | 0 | ir\_0-8->SE\_9 |
| 1 | 1 | T2\_update (from PE) |

**Reg T3:(2 control bits)**

En\_t3: Active high

t3\_1:

0->mem\_d

1->rf\_d1

**Reg T4: (1 control bit)**

En\_t4: Active high

**Flag Register:(2 control bit)**

flagz\_en: Active high

Flagc\_en: Active high

**Temporary zero register:(1 control bit)**

temp\_z\_en: Active high

**PC: (4 control bits)**

PC\_en: Active high

|  |  |  |  |
| --- | --- | --- | --- |
| pc\_1 | pc\_2 | pc\_3 | Mux\_pc o/p |
| 0 | 0 | 0 | alu\_out |
| 0 | 0 | 1 | rf\_d1 |
| 0 | 1 | 0 | t1 |
| 0 | 1 | 1 | t2 |
| 1 | 0 | 0 | t3 |
| 1 | 0 | 1 | ir0-8 -> LSHIFT 7 |

**IR (1 control bit)**:

IR\_en: active high

**Control word input order**

tempz| T4 | Current\_state | ir | carry\_reg | zero\_reg

**Control word output order**

alu\_op | alu\_amux | alu\_bmux | rf\_en | r7\_wr\_mux | rf\_a1\_mux | rf\_a3mux | rf\_d3mux | mem\_write\_bar | mem\_read\_bar | mem\_a\_mux | mem\_d1 | en\_t1 | t1\_mux | en\_t2 | t2\_mux | en\_t3 | t3\_1 | en\_t4 | flagz\_en | flagc\_en | PC\_en |PC\_mux| tempz\_en

IR order in input to control\_signal.vhd

17-14:Opcode

13-11:

10-8:ir6-8

7-5:IR3\_5

4-2:CZ